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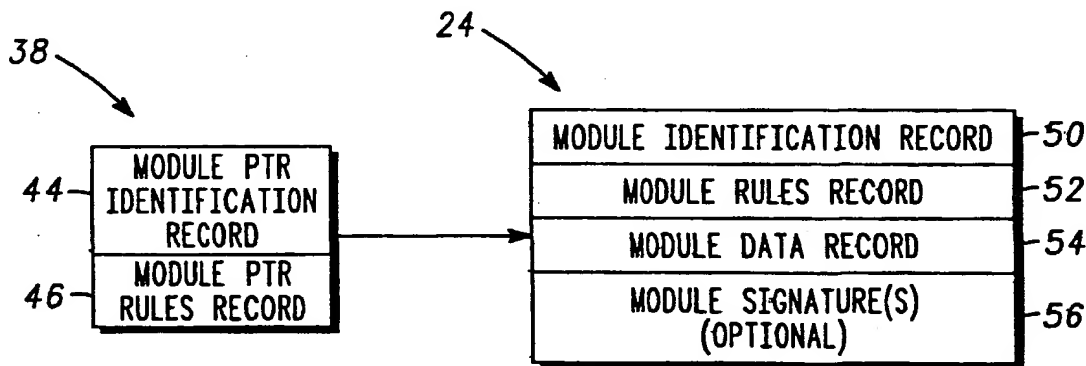
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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: SOFTWARE-DEFINED COMMUNICATIONS SYSTEM EXECUTION CONTROL



(57) Abstract: Software execution control in which a series of two-way rule checks is performed between software-defined communications system component records to ensure and maintain system security and integrity. A system platform (20) performs a series of two-way rule checks between records of a system platform (20) and an application (22) called by the platform (20), between records of the called application (22) and a module (24) that defines the called application (22), and between the records of the module (24) that defines the called application (22) and the platform (20). Both the called application (22) and the module (24) that defines the called application (22) are then instantiated if the two-way rule checks are successful. Because the rule checks are performed in a two-way manner, restrictions such as licensing and source restrictions may be placed not only on system modules (24-30), but also on the applications (22) using the modules (24-30), thereby enabling higher levels of system security to be achieved. In addition, the present invention minimizes processing overhead by providing for load-time rule checking rather than run-time checking associated with conventional enforcement systems.

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INTERNATIONAL SEARCH REPORT

Interni Application No
PCT/US 01/13374A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G06F1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 99 66387 A (L. GRÉGOIRE) 23 December 1999 (1999-12-23) the whole document	1-20
A	WO 97 07448 A (C. SIRBU) 27 February 1997 (1997-02-27) page 4, line 1 -page 7, line 31 page 12, line 18 -page 14, line 27 abstract; figures	1-20

☐ Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

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Date of the actual completion of the international search

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Soler, J

INTERNATIONAL SEARCH REPORT

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
WO 9966387	A	23-12-1999	WO 9966387 A1	23-12-1999
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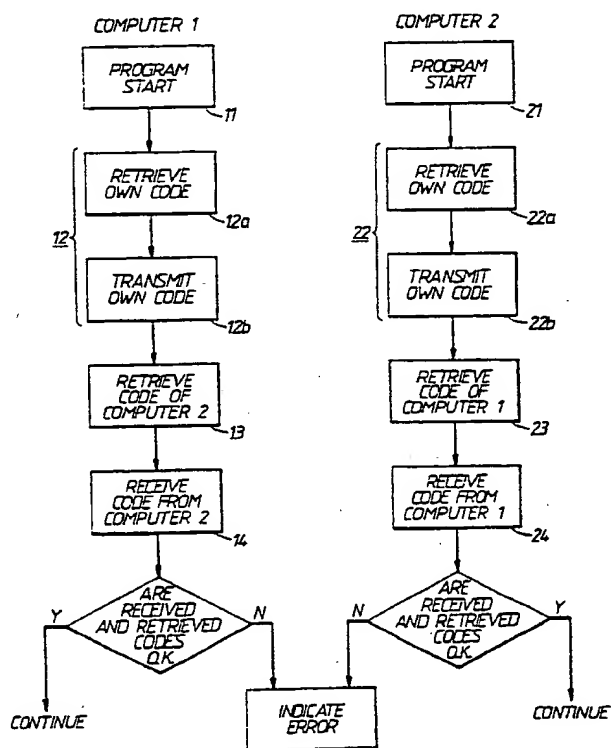
INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

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<p>(21) International Application Number: PCT/EP88/00502 (22) International Filing Date: 6 June 1988 (06.06.88) (71) Applicant (for all designated States except US): ROBERT BOSCH GMBH [DE/DE]; P.O. Box 50, D-7000 Stuttgart 1 (DE). (72) Inventors; and (75) Inventors/Applicants (for US only) : DROBNY, Wolfgang [DE/DE]; Flurweg 5, D-7122 Besigheim (DE). NITSCHKE, Werner [DE/DE]; Rosseger Weg 14, D-7257 Ditzingen 1 (DE). TAUFER, Peter [DE/DE]; Talstr. 45, D-7253 Renningen 2 (DE). WELLER, Hugo [DE/DE]; Moerikestr. 5, D-7141 Oberriexingen (DE). (81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent), US.</p>		<p>Published <i>With international search report.</i></p>

(54) Title: METHOD FOR MONITORING THE CORRECT COMBINATION OF PROCESSORS OR PROGRAMS IN A COMPUTER SYSTEM

(57) Abstract

A computer system incorporating two or more processors, each operating with a respective program, is arranged to monitor the processors and/or programs by assigning to each processor and/or program a unique identifying code. Each processor stores its own identifying code and the or each identifying code of associated processors. During initialisation the processors exchange identifying codes with each other, compare these and prevent operation of the system when the correct combination of processors and/or programs is not established.



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Method For Monitoring The Correct Combination
Of Processors Or Programs In A Computer System

The present invention relates to a system for ensuring that a correct system is being constructed during assembly of a computer system especially a safety system, incorporating two or more processors.

In many modern computer systems, particularly those using microprocessors, it is known to interconnect the microprocessors in order to achieve a desired overall function. In some applications, particularly where safety is involved, it is important to know that the correct parts have been used when building up the computer system as many of the parts are distinguishable only by careful inspection of code numbers on the parts or labels attached thereto.

The present invention proposes to overcome the difficulty of identification by an operator by inserting a so-called "code" in one processor and/or program associated with said one processor and a check "code" in another processor, and indicating when the "codes" do not correspond to alert an operator to incorrect assemble or faulty parts.

By the term "code" is meant any indication which is machine readable and is uniquely indicative of a processor or program.

In order that the present invention be more readily understood, an embodiment thereof will now be

described by way of example with reference to the accompanying drawing which shows a flow chart of the operation of a system according to the present invention.

If one considers the design of an electronic control device which utilizes two or more processors (CPU's) it is not uncommon for each processor to have associated therewith a program which is often stored in a ROM or PROM which may be on board or external. In order to ensure that the correct processors and programs are used in combination, each processor and/or program is assigned a unique identifying "code" and is also given the unique "code" of each associated processor and/or program which is to be connected to it. The processors then carry out a check on the identifying "code" and only if they correspond is the system acceptable.

This operation will be explained in more detail with reference to the drawing which assumes that there are only two processors involved. If one looks at the left side of the drawing processor 1 after program start at step 1, addresses the processor 2 at step 2 and processor 2 in turn transmits to processor 1 the identifying "code" of processor 2. Processor 1 also retrieves from its own memory at step 3 the stored identifying "code" of processor 2. When the transmitted "code" from processor 2 is received by processor 1 at step 4 the stored and transmitted "codes" are compared at step 5 and if they correspond the system is allowed to continue as indicated by a Y output. If the "codes" do not correspond an N output is generated at step 5 and an error is indicated at step 6 and if necessary to system is disabled.

As part of the addressing operation in step 2, the processor preferably retrieves its own identifying "code" at step 2a and transmits this at step 2b as the address to processor 2.

The right hand side of the drawing is identical to the left hand side and shows that processor 2 goes through the same steps as processor 1 and the steps, in relation to processor 2 are identified by similar reference numerals but increased by ten.

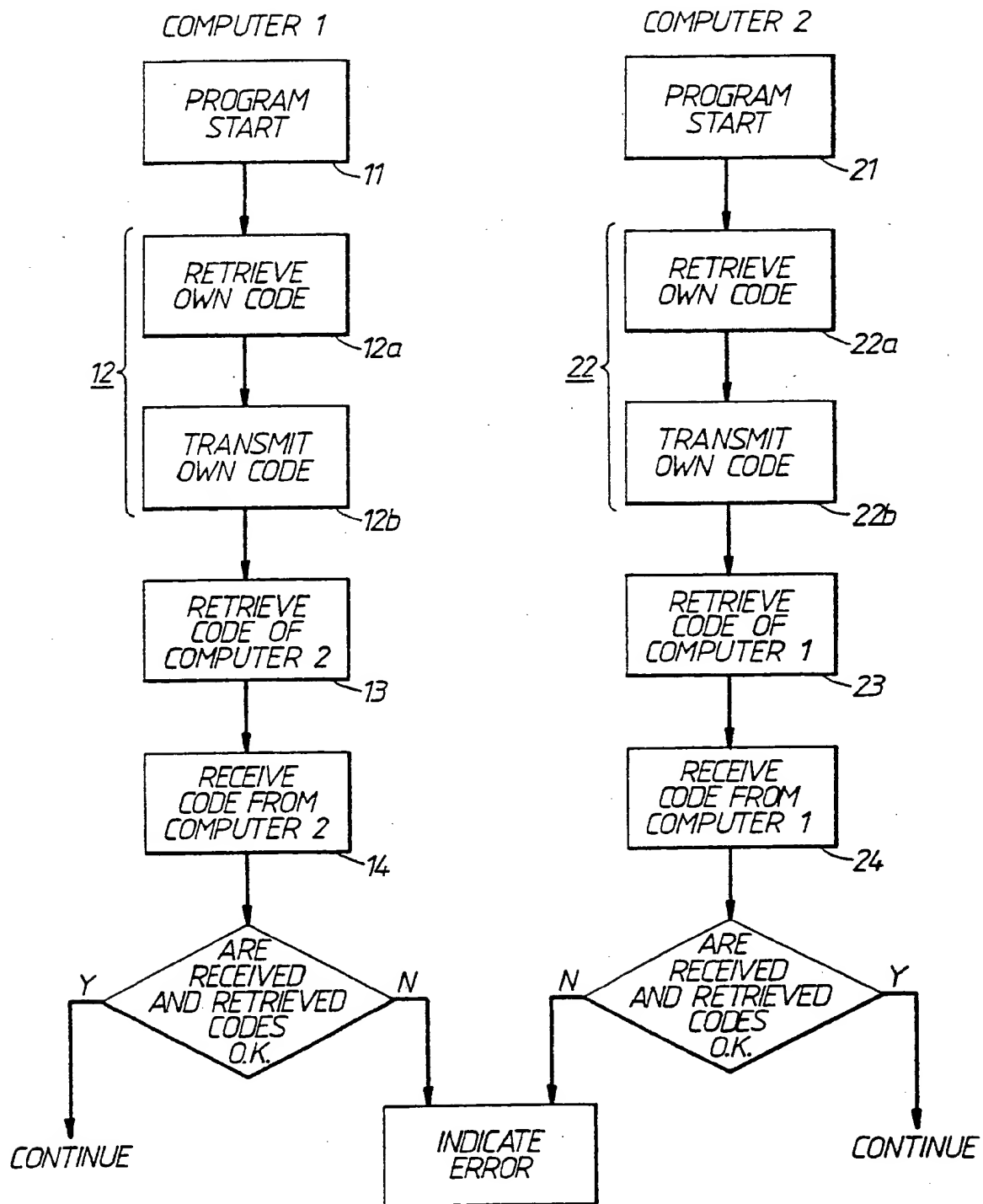
Although the identifying "code" is associated with a respective processor, it may indicate not only the processor but also the program or version of the program which that processor is using. This is particularly useful where updates in programs are taking place as it ensures that only correct function combinations of processors and/or programs are accepted. In this case, it is useful if the identification "name" is stored in EPROM in the processors involved as this permits easy modification. If no modifications are envisaged, the "name" may be stored in ROM.

The above operation is carried out during initialisation and the addressing and checking operation may take place only once or a predetermined number of times before the system is inhibited.

CLAIMS:


1. A method for monitoring a plurality of processors or programs in combination in a computer system comprising the steps of coupling at least two processors together to enable transfer of data and addresses therebetween, storing in each processor respective code identifying the processor and/or program used by the processor, storing in each processor a further code identifying the or each processor or program coupled thereto, causing each processor to address the or each processor coupled thereto, each addressed processor being arranged to transmit its respective identifying code to the addressing processor which compared each transmitted identifying code with its stored further codes and indicating when the transmitted codes do not correspond with the stored further codes.
2. A method according to claim 1, wherein the addressing step is carried out by sending each processor its own identifying code.
3. A method according to claim 1 or 2, wherein the indication that the transmitted codes do not correspond is that operation of the computer system is inhibited.

1/1



INTERNATIONAL SEARCH REPORT

International Application No PCT/EP 88/00502

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) ⁶		
According to International Patent Classification (IPC) or to both National Classification and IPC		
IPC ⁴ : G 06 F 15/16; G 06 F 11/00		
II. FIELDS SEARCHED		
Minimum Documentation Searched ⁷		
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IPC ⁴	G 06 F 15/16; G 06 F 11/00	
Documentation Searched other than Minimum Documentation to the extent that such Documents are included in the Fields Searched ⁸		
III. DOCUMENTS CONSIDERED TO BE RELEVANT ⁹		
Category ¹⁰	Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹²	Relevant to Claim No. ¹³
Y	Research Disclosure, no. 272, December 1986, (New York, US), "An efficient fault-tolerant membership protocol", page 745, disclosure no. 27257, see page 745, column 1 --	1,2
Y	Patent Abstracts of Japan, volume 9, no. 299 (P-408)(2022), 27 November 1985, & JP, A, 60135777 (FANUC K.K.) 19 July 1985 siehe das ganze Dokument --	1,2
Y	Automation and Remote Control, volume 34, no. 4,I, April 1973, Consultants' Bureau, a division of Plenum Publ., Corp., (New York, US), G.G. Stetsyura: "Large-scale systems and operations management decentralized coalitional control in data processing systems", pages 573-580 see page 577, lines 1-17; figure 1 -----	1,2
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IV. CERTIFICATION		
Date of the Actual Completion of the International Search		Date of Mailing of this International Search Report
31st January 1989		22.02.89
International Searching Authority EUROPEAN PATENT OFFICE		Signature of Authorized Officer  P.C.G. VAN DER PUTTEN

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